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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/716,479

11/20/2003

Hiroshi Kurakane

Q78541

6847

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EXAMINER

TRUONG, THANHNGA B

ART UNIT

PAPER NUMBER

2135

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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3 MONTHS

02/22/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/716,479	KURAKANE, HIROSHI	
	Examiner	Art Unit	
	Thanhnga B. Truong	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 November 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Thanhnga B. Truong
AU2135

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>11/20/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is responsive to the communication filed on November 20, 2003. Claims 1-8 are pending. At this time, claims 1-8 are rejected.

Information Disclosure Statement

2. The information disclosure statement (IDS) filed on November 20, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed on November 20, 2003.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okubo (US 7,000,140 B2), and further in view of Conviser (US 4,434,696).

a. *Referring to claim 1:*

i. Okubo teaches a clock control system (see Figure 1 of Okubo) comprising:

(1) a CPU, a peripheral functional block for said CPU
(column 4, lines 58-65 of Okubo),

(2) a frequency multiplication circuit which multiplies a frequency of an input system clock and outputs the multiplied system clock (see Figure 1, element 11 and column 4, line 60 of Okubo),

(3) a first frequency division circuit which divides a frequency of a signal output from said frequency multiplication circuit to generate a first

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clock to be supplied to said CPU (**see Figure 2 and more details in column 6, lines 48-55 of Okubo**),

(4) a second frequency division circuit which divides the frequency of the signal output from said frequency multiplication circuit to generate a second clock to be supplied to said peripheral functional block (**see Figure 2 and more details in column 6, lines 48-55 of Okubo**), and

(5) clock control means for changing a frequency multiplication ratio of said frequency multiplication circuit to $1/N$ (positive integer) and then changing a frequency division ratio of said frequency division circuit arranged on an input stage of said peripheral functional block to $1/N$ in order to set said CPU to a low-power consumption mode using no first clock (**column 1, lines 11-30 and lines 43-56 of Okubo**).

ii. Although Okubo teaches clock control circuit as shown in Figure 1 and the operation of PLL (phase-locked loop) circuit for multiplying a frequency provided in the clock pulse generator, Okubo is silent on the capability of showing the change frequency multiplication ratio of PLL to $1/N$. On the other hand, Conviser teaches this ratio of PLL to $1/N$ (**column 5, lines 34-47 of Conviser**).

iii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to:

(1) have modified the invention of Okubo with the teaching of Conviser to provide a ratio of the output of the PLL to the input of the modulo-N counter of M/N (**column 5, lines 46-48 of Conviser**).

iv. The ordinary skilled person would have been motivated to:

(1) have modified the invention of Okubo with the teaching of Conviser to provide all of the required frequencies of the equally-tempered scale base on the 12th root of 2 and exponents thereof for as many octaves as desired (**column 4, line 66 through column 5, line 2 of Conviser**).

b. Referring to claim 2:

i. The combination of teaching between Okubo and Conviser teaches the clock control circuit. They further teaches:

(1) wherein in order to cancel the low-power consumption mode of said CPU, said clock control means changes N times the frequency division ratio of said frequency division circuit arranged on the input stage of said peripheral functional block, and then changes N times the frequency multiplication ratio of said frequency multiplication circuit (**column 1, lines 11-30 of Okubo; and column 5, lines 40-47 of Conviser**).

c. Referring to claims 3-8:

i. These claims have limitations that is similar to those of claims 1 and 2, thus they are rejected with the same rationale applied against claims 1 and 2 above.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Ishimi (US 6,771,100 B2) discloses clock control circuit (see title).

b. Casal et al (US 5,524,035) discloses Symmetric clock system for a data processing system including dynamically switchable frequency divider (see title).


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhnga (Tanya) Truong whose telephone number is 571-272-3858.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached at 571-272-3859. The fax and phone numbers for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

TBT

February 15, 2007


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